LESSON PLAN 3rd sem DIGITAL ELECTRONICS AND COMPUTER ORGANISATION

Government Polytechnic, Balangir

Department of Computer Science Engineering

LESSON PLAN 2026-27(WINTER)

NAME OF THE TEACHER : DEEPAK KUMAR BARDA, LECT.CSE(STAGE-||)

Subject: **DIGITAL ELECTRONICS AND COMPUTER ORGANISATION** (Course Code: CSEPC 207/TH4)
Program: Diploma in Computer Science and Engineering
Semester: 3rd
Total Contact Hours: 45
Total Marks: 100
Assessment: Internal Assessment – 30, End Term – 70

After completion of the course, the students will be able to:
CO1: Define key concepts of digital electronics, including number systems, Boolean algebra, and logic gates.
CO2: Explain the principles behind combinational and sequential circuits, such as multiplexers, flip-flops, and counters, and their applications.
CO3: Implement simplified logic circuits using Karnaugh Maps and Boolean algebra to solve real-world digital design problems.
CO4: Analyze the instruction cycle, memory organization, and processor architecture to evaluate system performance and identify bottlenecks.
CO5: Design to simulate a basic CPU operation or create a functional digital circuit using the concepts of digital electronics and computer organization.

Period	Unit	Topic / Sub-Topic	Learning Objectives	Activity	Course Outcome	Learning Methodology	Homework
1	I	Difference Between Analog and Digital Signals	Differentiate between continuous and discrete signals.	Waveform drawing	CO1	Lecture & Visuals	Read chapter introduction on digital signals.
2	I	Number Systems: Binary, Octal, Decimal, Hexadecimal	Identify base values and representations for different number systems.	Concept Mapping	CO1	Lecture & Discussion	Write 1-20 in all four number systems.
3	I	Conversion Between Number Systems	Calculate equivalent values across different bases.	Group Calculation	CO1	Problem Solving	Complete 10 base conversion exercises.
4	I	Binary Arithmetic: Addition & Subtraction	Execute fundamental binary arithmetic operations.	Board Work	CO1	Demonstration	Solve 5 binary addition/subtraction problems.
5	I	Binary Arithmetic: Multiplication & Division	Execute complex binary arithmetic operations.	Peer verification	CO1	Problem Solving	Solve 5 binary multiplication problems.
6	I	Boolean Algebra: Basic Operations	Define logical AND, OR, NOT mathematically.	Truth Table creation	CO1	Lecture & Demo	Create truth tables for basic operations.
7	I	Boolean Algebra: Laws	Apply Commutative, Associative, and De Morgan's laws.	Proof tracing	CO1	Lecture	Memorize standard Boolean laws.
8	I	Boolean Algebra: Simplification	Reduce Boolean expressions to minimal forms.	Dry Run Exercises	CO1	Problem Solving	Simplify 3 provided Boolean expressions.
9	II	Logic Gates: AND, OR, NOT	Construct basic gate logic and truth tables.	Circuit sketching	CO1	Lecture & Visuals	Draw basic gate symbols and tables.

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10	II	Logic Gates: NAND, NOR	Explain the concept of universal gates.	Universal gate derivation	CO1	Demonstration	Implement an AND gate using only NAND gates.
11	II	Logic Gates: XOR, XNOR	Identify exclusive logic operations and their use cases.	Scenario Analysis	CO1	Lecture	Write truth tables for XOR/XNOR.
12	II	Design & Simplification using Boolean Algebra	Translate algebraic equations into logic circuit diagrams.	Whiteboard design	CO3	Problem Solving	Draw a circuit for a given Boolean equation.
13	II	Karnaugh Maps (K-Maps) Basics	Map truth tables onto 2 and 3-variable K-Maps.	Grid mapping	CO3	Demonstration	Map 2 standard expressions onto K-Maps.
14	II	K-Maps for Simplification (4-variable)	Group cells to extract simplified Boolean expressions.	Grouping Exercise	CO3	Problem Solving	Simplify a 4-variable expression using a K-Map.
15	II	Practical Applications in Real-World Circuits	Relate logic gates to daily electronic operations (e.g., alarms).	Brainstorming	CO1, CO3	Discussion	Identify one real-world use of an XOR gate.
16	III	Combinational Circuits: Multiplexers	Describe the data selector function of a MUX.	Block diagram sketching	CO2	Lecture & Visuals	Draw a 4-to-1 MUX block diagram.
17	III	Combinational Circuits: Demultiplexers	Contrast MUX data selection with DEMUX data distribution.	Concept Comparison	CO2	Demonstration	Draw a 1-to-4 DEMUX diagram.
18	III	Encoders and Decoders	Explain binary translation for I/O lines.	Truth table mapping	CO2	Lecture	Outline the difference between Encoders and Decoders.
19	III	Sequential Circuits: Intro & SR Flip-Flops	Differentiate combinational (no memory) and sequential (memory) circuits.	State simulation	CO2	Lecture & Demo	Create a truth table for an SR Flip-Flop.
20	III	Flip-Flops: JK, D, T	Explain race-around condition and data/toggle operations.	State transition tracing	CO2	Problem Solving	Compare the T and D flip-flop functions.
21	III	Synchronous Counters	Trace clock pulses triggering simultaneous state changes.	Timing diagram analysis	CO2	Demonstration	Sketch a basic timing diagram for a counter.
22	III	Asynchronous Counters	Explain ripple effects in cascaded flip-flops.	Output prediction	CO2	Lecture & Visuals	Read textbook chapter on ripple counters.
23	III	Registers and Shift Registers: Types and Uses	Model data storage and lateral data movement (SISO, PIPO).	Data flow drawing	CO2	Problem Solving	Trace a 4-bit serial shift operation.
24	IV	Basic Structure of a Computer: CPU, Memory, I/O	Identify the primary hardware components of a system architecture.	Architecture block diagram	CO4	Lecture & Discussion	Draw the Von Neumann architecture block.

25	IV	Instruction Cycle: Fetch	Outline how a CPU retrieves an instruction from memory.	Step-by-step tracing	CO4	Demonstration	Write out the fetch cycle micro-operations.
26	IV	Instruction Cycle: Decode & Execute	Explain how operations are interpreted and processed by the ALU.	Flowchart creation	CO4	Lecture	Create a complete fetch-decode-execute flowchart.
27	IV	Memory Organization: Types (RAM, ROM)	Differentiate volatile and non-volatile primary storage.	Concept Mapping	CO4	Lecture	List 3 differences between SRAM and DRAM.
28	IV	Memory Organization: Cache	Explain the principle of locality and speed bridging.	Access time calculation	CO4	Demonstration	Read about L1 vs L2 cache speeds.
29	IV	Memory Organization: Virtual Memory	Describe paging and logical-to-physical address translation.	Diagram mapping	CO4	Lecture & Visuals	Write a summary of why virtual memory is needed.
30	IV	Introduction to Buses: Address and Data Bus	Specify the direction and role of data/address transmission.	Bus width calculation	CO4	Demonstration	Calculate memory capacity based on address bus width.
31	IV	Introduction to Buses: Control Bus	Identify signals required to coordinate hardware timing.	System integration map	CO4	Problem Solving	List standard control signals (Read/Write, etc.).
32	V	Intro to Microprocessors & Microcontrollers	Contrast general-purpose processors with task-specific controllers.	Tech Spec comparison	CO4	Lecture & Discussion	Compare specs of a common PC vs an embedded device.
33	V	Basics of Arithmetic Logic Unit (ALU)	Detail the internal data paths for arithmetic and logic execution.	Block mapping	CO4	Demonstration	Draw a simplified ALU structural diagram.
34	V	Basics of Control Unit (CU)	Explain how timing signals direct ALU and memory operations.	Signal tracing	CO4	Lecture	Read chapter on Hardwired vs Microprogrammed CUs.
35	V	Instruction Set Architecture (ISA): Intro	Define the software-hardware interface boundary.	Opcode analysis	CO4	Problem Solving	Define opcode and operand formats.
36	V	RISC vs CISC Architecture	Compare Reduced vs Complex instruction sets regarding cycles and memory.	Chart generation	CO4	Lecture	Create a comparison chart for RISC and CISC.
37	V	Pipelining in Processors	Model instruction overlap to increase CPU throughput.	Pipeline simulation (Stages)	CO4	Demonstration	Draw a 4-stage pipeline execution diagram.
38	V	Performance Optimization	Evaluate hazards (data, structural, control) that slow down pipelining.	Bottleneck identification	CO4	Problem Solving	Review notes on pipeline hazards.

39	VI	I/O Devices and Interfaces (Keyboard, Mouse, Printers, Storage)	Map the peripheral connection logic to the main system.	Interface mapping	CO4	Lecture	Briefly explain how a keyboard sends a signal.
40	VI	Interrupts	Describe how external hardware commands CPU attention.	Flow control tracing	CO4	Demonstration	Differentiate maskable and non-maskable interrupts.
41	VI	Direct Memory Access (DMA)	Explain bypassing the CPU for bulk I/O memory transfers.	DMA cycle simulation	CO4	Lecture & Visuals	Draw a block diagram of a DMA controller.
42	VI	Modern Trends: Multicore Processors	Discuss parallel processing on a single chip.	Architecture review	CO4	Discussion	Read an article on dual-core vs quad-core CPU scaling.
43	VI	GPUs and Embedded Systems	Contrast serial processing (CPU) with parallel graphics processing (GPU).	Spec analysis	CO4	Lecture	Identify where embedded systems are used in cars.
44	VI	Mini-Project Prep: Design a Simple Digital Circuit	Apply Unit II and III concepts to sketch a functional circuit.	Project Workshop	CO5	Project-Based	Finalize logic diagram for the mini-project.
45	VI	Mini-Project: Simulate Basic CPU Operation	Synthesize the instruction cycle concepts into a simulated model.	Presentation / Review	CO5	Demonstration	Submit final mini-project documentation and review for exam.

Deepak kumar Barik
25.06.2026
Signature of Teacher

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